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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,327	02/11/2004	Jun Koyama	0756-7255	8544

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/775,327	KOYAMA ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2-37 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-37 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/309,891.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02-11-2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the preliminary amendment filed December 16, 2004.

Priority

This application filed under former 37 CFR 1.60 lacks the necessary reference to the prior application. A statement reading "This is a Divisional of Application No. 09/309,891, filed May 11, 1999." should be entered following the title of the invention or as the first sentence of the specification. Also, the current status of all nonprovisional parent applications referenced should be included.

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/309,891, filed on May 11, 1999.

Specification

The abstract of the disclosure is objected to because "**comprises**" should have been **includes** in line 4. Correction is required. See MPEP § 608.01(b).

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-9 and 30-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama et al. (5,977,940).

In regard to claim 2, Akiyama et al. teach a semiconductor device comprising: a plurality of pixels over a substrate; a data line driver circuit over the substrate; and a dividing circuit over the substrate (Figures 1A; columns 9, 10, 12, 15 and 19; lines 28-37, 14-22 & 29-35, 23-36, 1-6 and 41-51, respectively).

In regard to claim 3, Akiyama et al. teach a semiconductor device comprising: a plurality of pixels over a substrate; a data line driver circuit comprising a plurality of NAND circuits over the substrate; and a dividing circuit over the substrate (Figures 1A; columns 9, 10, 12, 14, 15 and 19; lines 28-37, 14-22 & 29-35, 23-36, 35-50, 1-6 and 41-51, respectively).

In regard to claim 4, Akiyama et al. teach a semiconductor device comprising: a plurality of pixels over a substrate; a data line driver circuit over the substrate; a dividing circuit over the substrate (Figures 1A; columns 9, 10, 12, 15 and 19; lines 28-37, 14-22 & 29-35, 23-36, 1-6 and 41-51, respectively).

In regard to claim 5, Akiyama et al. teach a semiconductor device comprising: a plurality of pixels over a substrate; a data line driver circuit comprising a plurality of

NAND circuits over the substrate; and a dividing circuit over the substrate (Figures 1A; columns 9, 10, 12, 14, 15 and 19; lines 28-37, 14-22 & 29-35, 23-36, 35-50, 1-6 and 41-51, respectively).

In regard to claim 6, Akiyama et al. teach a semiconductor device comprising: a plurality of pixels over a substrate, each of the plurality of pixels having a thin film transistor; a data line driver circuit over the substrate; and a dividing circuit over the substrate (Figures 1A; columns 9, 10, 12, 15 and 19; lines 28-37, 14-22 & 29-35, 23-36, 1-6 and 41-51, respectively).

In regard to claim 7, Akiyama et al. teach a semiconductor device comprising: a plurality of pixels over a substrate, each of the plurality of pixels having a thin film transistor; a data line driver circuit comprising a plurality of NAND circuits over the substrate; and a dividing circuit over the substrate (Figures 1A; columns 9, 10, 12, 14, 15 and 19; lines 28-37, 14-22 & 29-35, 23-36, 35-50, 1-6 and 41-51, respectively).

In regard to claim 8, Akiyama et al. teach a semiconductor device comprising: a plurality of pixels over a substrate, each of the plurality of pixels having a thin film transistor; a data line driver circuit over the substrate; a dividing circuit over the substrate (Figures 1A; columns 9, 10, 12, 14, 15 and 19; lines 28-37, 14-22 & 29-35, 23-36, 35-50, 1-6 and 41-51, respectively).

In regard to claim 9, Akiyama et al. teach a semiconductor device comprising: a plurality of pixels over a substrate, each of the plurality of pixels having a thin film transistor; a data line driver circuit comprising a plurality of NAND circuits over the

substrate; and a dividing circuit over the substrate (Figures 1A; columns 9, 10, 12, 14, 15 and 19; lines 28-37, 14-22 & 29-35, 23-36, 35-50, 1-6 and 41-51, respectively).

In regard to claims 30-37, Akiyama et al. teach the semiconductor device applied to a personal computer (columns 1 and 2-3; lines 16-18, 66-67 and 1-2, respectively).

However, Akiyama et al. fail to explicitly teach the various functions of the dividing circuit.

In regard to the dividing circuit dividing a signal into n signals, wherein the n signals inputted into corresponding n pixels by a timing signal supplied from the data driver circuit, simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the dividing circuit dividing a signal into n signals, wherein the n signals inputted into corresponding n pixels by a timing signal supplied from one of the plurality of NAND circuits, simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the dividing circuit dividing three signals corresponding to colors R, G and B into 3n signals, wherein the 3n signals are inputted into corresponding 3n pixels

by a timing signal supplied from the data driver circuit, simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the dividing circuit dividing three signals corresponding to colors R, G and B into 3n signals, and wherein the 3n signals are inputted into corresponding 3n pixels by a timing signal supplied from one of the plurality of NAND circuits, simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the dividing circuit dividing a signal into n signals, and wherein the n signals are inputted into thin film transistors corresponding n pixels by a timing signal supplied from the data driver circuit, simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the dividing circuit dividing a signal into n signals, and wherein the n signals are inputted into thin film transistors corresponding to n by a timing signal

supplied from one of the plurality of NAND circuits, pixels simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the dividing circuit dividing three signals corresponding to colors R, G and B into 3n signals, wherein the 3n signals are inputted into thin film transistors corresponding to 3n pixels by a timing signal supplied from the data driver circuit, simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the dividing circuit dividing three signals corresponding to colors R, G and B into 3n signals, and wherein the 3n signals are inputted into thin film transistors corresponding to 3n by a timing signal supplied from one of the plurality of NAND circuits, pixels simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was for the semiconductor device structure as taught by Akiyama et al. to perform the various functions of the dividing circuit to provide a liquid crystal display device that consumes less power.

Claims 10-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama et al. (5,977,940) as applied to claims 2-9 and 30-37 above, and further in view of Yamazaki (6,115,097).

Akiyama et al. teach all mentioned in the rejection above.

However, Akiyama et al. fail to teach the data line driver circuit comprising a shift register, NAND circuits, a level shifter and a buffer; the substrate comprising glass; and the thin film transistor comprising polycrystalline silicon film.

Yamazaki teaches a data line driver circuit comprising a shift register, NAND circuits, a level shifter and a buffer (column 10, lines 33-36); a substrate 401 comprising glass (Figure 4A, column 3, lines 51-54); and a thin film transistor comprising polycrystalline silicon film (column 1, lines 26-29).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was modify the semiconductor device structure as taught by Akiyama et al. with the semiconductor device having a data line driver circuit comprising a shift register, NAND circuits, a level shifter and a buffer; and a substrate comprising glass as taught by Yamazaki to provide a semiconductor device capable of being used

as a display of portable video cameras and portable business equipment, and further of various types of information terminal equipment (column 1, lines 44-52).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor display devices:

Furuhashi et al. (US 2002/0154086 A1)

Kikuo et al. (5,250,937)

Kwon (5,850,216)

Sato et al. (5,712,652)

Yokota et al. (US 2004/0160398 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
September 18, 2005

John M. Howard
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